**Chapter 4.**

Problem 1.

When access time of Main Memory is 3500 ns and Cache Memory is 125 ns and miss ratio is 0.3. Calculate the average access time of CPU?

Miss ratio + hit ratio = 1

Average access time = Access time of CM \* hit ratio + Access time of MM \* miss ratio

=125\*0.7 + 3500\*0.3

= 1137.5 ns

**Problem 4.1**

**A** set-associative cache consists of 64 lines, or slots, divided into four-line sets. Main memory contains 4K blocks of 128 words each. Show the format of main memory addresses**.**

**Answer:**

Number of sets = 64/4 = 16

=> The cache is divided into 16(= 2⁴) sets

Therefore, 4 bits are needed to identify the set number.

To represent 16 we need = 4 bits

Main memory consists of 4K = 2¹² blocks.

Block number = Set number + Tag number

Set is the part of block

Tag is also a part of block

Therefore, the set + tag lengths must be 12 bits

Tag length = 12 - 4 = 8

Each block contains 128 words = 2⁷ words

Therefore, 7 bits are needed to specify the word field

So, the main memory can be represented as

TAG SET WORD

8 4 7

**Problem 4.2**

A two-way set-associative cache has lines of 16 bytes and a total size of 8 Kbytes. The 64-Mbyte main memory is byte addressable. Show the format of main memory addresses.

**Answer:**

* Two way set associative mapping.
* Size of each cache line = 16 bytes
* Size of cache memory = 8 KB
* Number of Blocks at the cache = 8192 byte/16byte=512 blocks (lines in the cache)
* It is two way associative, so the cache consists of 2 sets
* Each set consists of =512/2=256 sets of 2 line each
* Number of bits required for “SET field” in main memory address format is 8-bit

(Because 2^8=256)

Set number is =8

Main memory 64 M byte= 2^ 26 (26-bit address memory)

* Number of Blocks at the Memory= 64 M byte/16 byte=4 M blocks=2^22
* So, the number of blocks is = 22

We know, Block number = Set number + Tag number

Thus, Tag field =22 - 8=14 bits

The remains will be the Word length or

Block size=16 byte= 2^4 (Word length = 4)

TAG SET WORD

14 8 4

**Set:**

**Main memory = Hard disk and cache memory**

**To represent CM we use SET**

**To represent HD we use TAG**

**Block of main memory = Set + Tag**

**4.8 Consider a machine with a byte addressable main memory of 2^16 bytes and block size of 8 bytes. Assume that a direct mapped cache consisting of 32 lines is used with this machine.**

1. How is a 16-bit memory address divided into tag, line number, and byte number?
2. Into what line would bytes with each of the following addresses be stored?

0001 0001 0001 1011

1100 0011 0011 0100

1101 0000 0001 1101

1010 1010 1010 1010

1. Suppose the byte with address 0001 1010 0001 1010 is stored in the cache. What are the addresses of the other bytes stored along with it?
2. How many total bytes of memory can be stored in the cache?
3. Why the tag is also stored in the cache?

Ans.

a)

Address length: 16 bits

Word: 3 rightmost bits (as the block size if 8 bytes)

Line: 5 middle bits (as there are 32 lines)

Tag: 8 leftmost bits (as 16 – 3 – 5=8)

b)

0001 0001 0001 1011 →  line 3

1100 0011 0011 0100 →  line 6

1101 0000 0001 1101 →  line 3

1010 1010 1010 1010 →  line 21

c)

Bytes with addresses

0001 1010 0001 1000

0001 1010 0001 1001

0001 1010 0001 1010

…

0001 1010 0001 1111

are stored in the cache.

d)

32 lines \* 8 bytes = 256 bytes

e)

It is because 2 items with two different memory addresses can be stored in the same place in the cache. The tag is used to distinguish between them.

**4.19 Consider a memory system with the following parameters:**

**Tc = 100 ns Cc = 10^-4 $/ bit**

**Tm = 1200 ns Cm = 10^-5 $/ bit**

a. What is the cost of 1 MByte of main memory?

b. What is the cost of 1 MByte of main memory using cache memory technology?

c. If the effective access time is 10% greater than the cache access time, what is the hit ratio H?

Ans:

1 MB = 1024 KB = 1024\*1024\*8 = 8388608 bits\*10^-5= 83.88 $

1 Kbit = 1000 bit

1MBytes=8000000 = 8X10**^**6 bit

1GBytes=8000000000 = 8X10**^**9 bit

a.

Cost = Cm \* 1 MB = 10**^-5** \* 8 \* 10**^**6 $ = 80 $ = $80

b.

Cost = Cc \* 1 MB = 10**^-4** \* 8 \* 10**^**6 $= 800 $ = $800

C.

**Effective Access Time:**  
Te = H x Tc + (1 - H)(Tm + Tc),  
Tc access time of cache

Tm access time of main  
Tc = 100ns,  
Te = 1.1 x Tc  
Tm = 1200ns.  
  
Thus,  
(1.1) x (100) = H x 100 + (1 - H) (1200 + 100)  
110 = 100H + 1300 - 1300H  
H = 1190/1200

**Chapter 5.**

**Problem 5.1**

Consider a dynamic RAM that must be given a refresh cycle 64 times per ms. Each refresh operation requires 150 ns; a memory cycle requires 250ns. What percentage of the memory’s total operating time must be given to refreshes?

Solution:

In 1 ms, the time devoted to refresh is 64 \* 150 ns = 9600 ns

The fraction of time devoted to memory refresh is = (9600\*1000)/109 s = 9.6\*10-3s =0.0096

which is approximately 1%.

**Problem 5.3**

Assume that the access time is 60ns and the recharge time is 40ns.

1. What is the memory cycle time? What is the maximum data rate this DRAM can sustain, assuming a 1-bit output?
2. Constructing a 32-bit memory system using these chips yields what data transfer rate?

**Solution a:**

Memory cycle time = (60 + 40) ns = 100 ns

Therefore, the maximum data rate is 1 bit in every 100 ns,

100 ns = 1 bit

which is 10 Mbps

**Solution b:**

If 1 bit in every 100ns then

For 32-bit memory system data rate is = 32\* 10 Mbps = 320 Mbps

Which is 40 MB/s (MB/ second)

**Chapter 6.**

**6.2 Define the following for a disk system:**

**ts =seek time; average time to position head over track**

**r = rotation speed of the disk, in revolutions per second**

**n = number of bits per sector**

**N = capacity of a track, in bits**

**tA = time to access a sector**

**Develop a formula for tA as a function of the other parameters.**

Solution:

tA = ts + 1/2r + n/rN

**6.4 Consider a single-platter disk with the following parameters: rotation speed:**

**7200 rpm; number of tracks on one side of platter: 30,000; number of sectors per**

**track: 600; seek time: one ms for every hundred tracks traversed. Let the disk receive**

**a request to access a random sector on a random track and assume the disk head**

**starts at track 0.**

**a. What is the average seek time?**

**b. What is the average rotational latency?**

**c. What is the transfer time for a sector?**

**d. What is the total average time to satisfy a request?**

**Solution a:**

1. If the requested track is track 0, then the seek time is 0, if the requested track is track 29,999, then the seek time is the time to traverse 29,999 tracks. For a random request, on average the number of tracks traversed is 29,999/2 = 14999.5 tracks. At one ms per 100 tracks, the average seek time is therefore 149.995 ms.
2. At 7200 rpm, there is one revolution every 8.333 ms. Therefore, the average rotational delay is 4.167 ms.
3. With 600 sectors per track and the time for one complete revolution of 8.333 ms, the transfer time for one sector is 8.333 ms/600 = 0.01389 ms.

**d.** The result is the sum of the preceding quantities, which is 154.175 or approximately 154 ms.

**Q1. Consider a magnetic disk drive with 8 surfaces, 512 tracks per surface, and 64 sectors per track. Sector size is 1 KB. The average seeking time is 8 ms, the track to track access time is 1.5 ms, and the drive rotates at 3600 rpm. Successive tracks in a cylinder can be read without head movement.**

1. What is the disk capacity?
2. What is the average access time? Assume this file is stored in successive sectors and tracks of successive cylinders, starting at sector 0, track 0, of cylinder i.
3. Calculate the number of tracks, sectors, and cylinders for a 5 MB hard disk.

**Solution:**

1. Capacity = Surfaces x tracks x sectors x sector size  
   = 8 x 512 x 64 x 1KB = 262144 KB =256MB
2. Assume this file is stored in successive sectors and tracks of successive cylinders, starting at sector 0, track 0, of cylinder i.

3600 round in 60 sec

1 round in (60/3600) sec

Rotation time =60/3600 sec

Rotational latency= Rotation time/2 = 60/3600x2 = 8.3 m sec

Average Access time = Seek time + rotational delay + track to track access time.

= 8ms + 8.3ms + 1.5ms = 17.8ms

1. 5MB = 5242880 bytes.

5242880/1KB\*64 = 5242880 / 65536 = 80 tracks.

80 \* 64 = 5120 sectors.

So, 80 tracks, 5120 sectors, 10 cylinders (80 tracks / 8 surfaces)

Q2.

1. **A magnetic disk has an average seek time of 5 ms. The transfer rate is 50 MB/sec. The disk rotates at 10,000 rpm and the controller overhead is 0.2 ms. Find the average time to read or write 1024 bytes of data.**

**Solution:**

Average seek time=5ms

Average rotation time = 60/10000 sec

Rotational latency =0.5\*60/10,000=3 ms

Transfer time=1KB/50MB=0.02ms

Controller overhead =0.2ms

The total time taken= 5+3+0.02+0.2 =8.22 ms

1. A hard disk with 5 platters has 1024 tracks per platter, 512 sectors per track and 512 bytes/sector. Find the total capacity of the disk.

**Solution:**

**5 x 1024 x 512 x 512 = 1342177280 bytes = 1310720 KB =1280 MB=1.25 GB**

512 bytes x 512 sectors=0.2MB/track

0.2MB x 1024 tracks=0.2GB/platter

Therefore, the hard disk has the total capacity of 5 x 0.2=1.25 GB

1. Calculate how many platters are required for a 40GB disk if there are 1024 bytes/sector, 2048 sectors/track and 4096 tracks per platter

**Solution:**

The capacity of one platter = 1024 x 2048 x 4096 = 8GB

For a 40GB hard disk, we need 40/8 = 5 such platters

**Chapter 7.**

**Problem 7.12:**

**A DMA module is transferring characters to memory using cycle stealing from a device transmitting at 9600 bps. The processor is fetching instructions at the rate of 1 million instructions per second (1 MIPS). By how much will the processor be slowed down due to the DMA activity?**

Solution:

DMA module transferring characters at 9600 bps = 9600/8 Bps = 1200 Bps  
Processor is fetching instructions at the rate = 1 MIPS (million instruction per second)  
Slowdown = 1200\*100/106 = 0.12%

**Problem 7.14:**

Examination of the timing diagram of the 8237A indicates that once a block transfer begins, it takes three bus clock cycles per DMA cycle. During the DMA cycle, the 8237A transfers one byte of information between memory and I/O devices

1. Suppose we clock the 8237A at a rate of 5 MHz. How long does it take to transfer one byte?
2. What would be the maximum attainable data transfer rate?
3. Assume that the memory is not fast enough, and we have to insert two wait states per DMA cycle. What will be the actual data transfer rate?
4. At 5 MHz,

5 MHz means 5000000 cycles per second

So, 5000000 cycles takes 1 second

1 cycle takes=1/5000000 sec = 0.2 μs

So, the one clock cycle takes 0.2 μs.

A transfer of one byte takes 3\*0.2= 0.6μs because one DMA cycle takes three bus cycles

1. The data rate = 1/transfer rate = 1/(0.6 ×10-6 )=  
   =1.67 MB/s

0.6 μs needs to transfer 1 byte of data

0.6/1000000 sec needs to transfer 1 byte of data

So, 1 sec needs to transfer = 1\* 1000000/0.6 =1666666.667 bytes=1666.667=

1.5894 MB of data

1. Two wait states add an addition = (0.2 + 0.2) μs = 0.4 μs,

So, that a transfer of one byte takes= (0.4μs+0.6μs) =1μs.

1 μs need to transfer 1 byte of data

1/1000000 sec is required to transfer 1 Byte

1 sec required to transfer=1000000 Byte=1 MB

The resulting datarate= 1/((0.6+0.4)×10-6)=1/(1×10-6)  
=1MB/s

**Problem 7.15:**

**Assume that in the system of the preceding problem, a memory cycle takes 750 ns. To what value could we reduce the clocking rate of the bus without effect on the attainable data transfer rate?**

Solution:

A DMA cycle could take as long as 750/1000= 0.75 µs without the need for wait states.

This corresponds to a clock period of **0.75/3 = 0.25 µs,** which in turn corresponds to a clock rate of 4 MHz.

**Problem 7.16:**

**A DMA controller serves four receive-only telecommunication links (one per DMA channel) having a speed of 64 Kbps each.**

**a. Would you operate the controller in burst mode or in cycle-stealing mode? b. What priority scheme would you employ for service of the DMA channels?**

Solution:

**a.** Telecommunications links can operate continuously, so burst mode cannot be used, as this would tie up the bus continuously. Cycle-stealing is needed.

**b.** Because all 4 links have the same data rate, they should be given the same priority.

**Problem : 7.17**

A 32-bit computer has two selector channels and one multiplexor channel. Each selector channel supports two magnetic disk and two magnetic tape units. The multiplexor channel has two-line printers, two card readers, and 10 VDT terminals connected to it. Assume the following transfer rate:

Disk drive: 800 Kbytes/sec

Magnetic tape drive 200 Kbytes/sec

Line printer 6.6 Kbytes /sec

Card reader: 1.2 Kbytes/sec

VDT: 1 Kbytes/sec

Estimate the maximum aggregate I/O transfer rate in this system.

Selector selects one device at a time, Multiplexer for getting output from one or more than one device.  
For Selector I/O transfer rate = maximum of (two magnetic disk and two magnetic tape units) = max(800, 200) =800KBps

For two selector=800\*2=1600 KBps

For Multiplexer I/O transfer rate = 2\*6.6 + 2\*1.2 +10\*1 = 25.6Kbyte/sec

So , total maximum aggregate I/O transfer rate =  1600 + 25.6 =1625.6Kbyte/sec

**Example: A DMA controller transfers 32-bit words to memory using cycle stealing. The words are assembled from a device that transmits characters at a rate of 4800 characters per second. The CPU is fetching and executing instructions at an average rate of one million instructions per second. By how much will the CPU be slowed down because of the DMA transfer?**

Solution:

DMA controller transfers 32 bit(4 byte) words to memory(cycle stealing mode).  
Device transmits 4800 character per second (1 character = 1 byte)  
So, for 1 byte it will take 1 / 4800 sec.  
Since the controller transfers 4 byte in cycle stealing mode, it will take 4 \* (1 / 4800) = 1 / 1200 sec.  
So, 1200 characters will be transferred in cycle stealing mode and it is given that CPU is fetching and executing instructions at an average rate of one million instructions per second. Slow down or cycle wasted % in DMA transfer = (1200/1000000) \* 100 = 0.12 %